in response to receipt from the host processor of user data and a command to write said user data to said at least one mass memory storage block address, writing at least one sector of said user data into the addressed at least one of the memory array cell groups, and

in response to receipt from the host processor of a command to read user data from said at least one mass memory storage block address, reading at least one sector of said user data and associated overhead data from the addressed at least one of the memory array cell groups.

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32 ~~82~~. (Amended) A bulk storage memory system that is connectable to a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells arranged to store in designated [locations] blocks thereof [a plurality of blocks of] a given amount of user data and associated [units of] overhead data, and

a controller connectable to said computer system for controlling operation of the array, said controller including:

an addressing circuit responsive to receipt of a mass memory storage block address from the host computer system to address a corresponding array block of user data and [its] associated [unit of] overhead data,

a reading circuit responsive to the addressing circuit to read [a unit of] the associated overhead data [associated with] of the addressed array block [of user data], and

a [reading] data transfer circuit responsive to the addressing circuit and the read [unit of] overhead data to execute an instruction from the host computer system to perform a designated one of reading user data from, or writing user data to, the addressed [user data] array block.

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33 ~~83~~. (Twice Amended) The memory system according to claim 32 ~~82~~ additionally comprising a list of any of said [designated locations] blocks that are unusable that link said unusable [locations] blocks with others of said [locations] blocks that are usable, and wherein said addressing circuit includes a circuit to access linked others of said [locations] blocks in place of said unusable [locations] blocks.

34 ~~84~~. (Twice Amended) The memory system according to claim 33 ~~83~~ wherein the list of unusable [locations] blocks includes a list maintained within the bulk storage memory system outside of [locations] blocks of the memory array designated to store [blocks of] user data and associated [units of] overhead data.

35 ~~85~~. (Twice Amended) The memory system according to claim 33 ~~83~~ wherein the list of unusable [locations] blocks includes a list stored as part of [units of] the overhead data associated with the unusable [locations of the memory array] blocks.

-3

36 ~~86~~. (Twice Amended) The memory system according to any one of claims 33 ~~83~~-35 ~~85~~ wherein the list of any unusable [locations] blocks includes inoperable or defective [locations] blocks.

37 ~~87~~. (Twice Amended) The memory system according to any one of claims 33 ~~83~~-35 ~~85~~ wherein the list of any unusable [locations] blocks includes [locations] blocks that contain a number of defective cells in excess of a preset number.

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47 ~~93~~. (Twice Amended) The memory system according to any one of claims 32 ~~82~~-35 ~~85~~, wherein [individual blocks of user data and corresponding units of overhead data are stored together within individual ones of a plurality of locations of the memory cell array] the data transfer circuit additionally transfers user data in parallel to and from the host computer system.

-4

48 ~~94~~. (Twice Amended) The memory system according to any one of claims [93] 32 ~~82~~-35 ~~85~~, additionally comprising an erasing circuit that simultaneously erases the [individual] memory cells within individual designated [locations] array blocks to simultaneously erase any user data and associated [unit of] overhead data stored therein.

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53 ~~115~~. (Amended) A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion,

detecting a predefined condition when individual sectors become unusable and linking the addresses of such unusable sectors with addresses of other sectors that are useable,

causing the controller, in response to receipt from the processor of an address in a format designating at least one [magnetic disk sector] mass memory storage block, to generate an address of a non-volatile memory sector that corresponds to said at least one [magnetic disk sector] mass memory storage block,

accessing a usable sector of the memory system, if the sector with the generated address is unusable, by referring to the linked address of another sector that is usable and then accessing that other sector,

either writing data to, or reading data from, the user data portion of the accessed usable sector, and

either writing to, or reading from, said overhead portion of the accessed usable sector, information related to either the accessed usable sector or data stored in the user data portion of said accessed useful sector[, and

wherein writing to the accessed usable sector includes programming the individual memory cells thereof into one of more than two programmable states in order to store more than one bit of data or information per cell].

~~123~~. (Amended) The method according to claim ~~115~~, wherein causing the controller to generate an address of a non-volatile memory sector includes doing so for a non-volatile memory sector that corresponds to only one [magnetic disk sector] mass memory storage block, wherein the user data portion of the individual non-volatile memory sectors has a capacity that is substantially the same as a user data portion of said one [magnetic disk sector] mass memory storage block.

67
124. (Amended) A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion,

causing the controller, in response to receipt from the processor of an address in a format designating at least one [magnetic disk sector] mass memory storage block, to designate an address of at least one non-volatile memory sector that corresponds with said at least one [magnetic disk sector] mass memory storage block,

either writing user data to, or reading user data from, the user data portion of said at least one non-volatile memory sector, and

either writing to, or reading from, said overhead portion of said at least one non-volatile memory sector, overhead data related either to said at least one non-volatile memory sector or to data stored in the user data portion of said at least one non-volatile memory sector[, and

wherein writing to said at least one non-volatile memory sector includes programming the individual memory cells thereof into one of more than two programmable states in order to store more than one bit of data per cell].

Please add the following new claims:

62
~~131~~. The method of any one of claims ~~115~~53-~~123~~61, wherein writing to the accessed usable sector includes programming the individual memory cells thereof into exactly two programmable states in order to store exactly one bit of data or information per cell.

63 62
~~132~~. The method of claim ~~131~~, wherein the address of said at least one mass memory storage block is an address of at least one magnetic disk sector.

64 53 61
~~133~~. The method of any one of claims ~~115~~-~~123~~, wherein writing to the accessed usable sector includes programming the individual memory cells thereof into one of more than two programmable states in order to store more than one bit of data or information per cell.

65 64
~~134~~. The method of claim ~~133~~, wherein the address of said at least one mass memory storage block is an address of at least one magnetic disk sector.

66 53 61
~~135~~. The method any one of claims ~~115~~-~~123~~, wherein communication of mass memory storage block addresses and user data with the controller is in parallel over a bus.

74 67 73
~~136~~. The method of any one of claims ~~124~~-~~130~~, wherein writing to said at least one non-volatile memory sector includes programming the individual memory cells thereof into one of exactly two programmable states in order to store exactly one bit of data per cell.

75 74
~~137~~. The method of claim ~~136~~, wherein the address of said at least one mass memory storage block is an address of at least one magnetic disk sector.

76 67 73
~~138~~. The method of any one of claims ~~124~~-~~130~~, wherein writing to said at least one non-volatile memory sector includes programming the individual memory cells thereof into one of more than two programmable states in order to store more than one bit of data per cell.

77 76
~~139~~. The method of claim ~~138~~, wherein the address of said at least one mass memory storage block is an address of at least one magnetic disk sector.

78 67 73
~~140~~. The method any one of claims ~~124~~-~~130~~, wherein communication of mass memory storage block addresses and user data with the controller is in parallel over a bus.

79
~~141~~. A memory system connectable to a host processor to enable the exchange of data therebetween, said memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of blocks of cells that individually store a given amount of user data and overhead data, and

a controller connected to the array and removably connectable to the host through an electrical connector, said controller including:

an address generator that is responsive to receipt of a mass memory storage block address from the host to address a corresponding at least one of the plurality of memory blocks, and

a data transfer control that responds to an instruction from the host to perform a designated one of reading user data from, or writing user data to, said at least one addressed block, including a data writing circuit that generates at least some of the overhead data associated with at least one of at least one addressed block or user data being written therein, and a data reading circuit that reads the overhead data from said at least one addressed block.

80 79
142. The memory system according to claim 141 additionally comprising a list of any of said memory blocks that are unusable that link said unusable blocks with others of said blocks that are usable, and wherein said addressing circuit includes a circuit to access linked others of said blocks in place of said unusable blocks.

81 80
143. The memory system according to claim 142 wherein the list of unusable blocks includes a list maintained within the bulk storage memory system outside of blocks of the memory array designated to store user and overhead data.

82 80
144. The memory system according to claim 142 wherein the list of unusable blocks includes a list stored as part of the overhead data associated with unusable memory array blocks.

83 80 82
145. The memory system according to any one of claims 142-144 wherein the list of any unusable blocks includes inoperable or defective blocks.

84 80 82
146. The memory system according to any one of claims 142-144 wherein the list of any unusable blocks includes blocks that contain a number of defective cells in excess of a preset number.

85 ~~147.~~ The memory system according to any one of claims ~~141~~ 79 - ~~144~~ 82 wherein said given amount of user data is substantially 512 bytes.

86 ~~148.~~ The memory system according to any one of claims ~~141~~ 79 - ~~144~~ 82 wherein said mass memory storage block address is a magnetic disk sector address.

87 ~~149.~~ The memory system according to claim ~~148~~ 86 wherein said magnetic disk sector address includes a head, cylinder and sector.

88 ~~150.~~ The memory system according to any one of claims ~~141~~ 79 - ~~144~~ 82, wherein said bulk storage memory system is implemented in a single package.

89 ~~151.~~ The memory system according to claim ~~150~~ 88, wherein said bulk storage memory system is provided within a card that is removably connectable to the computer system through said electrical connector.

E7

92 ~~152.~~ The memory system according to any one of claims ~~141~~ 79 - ~~144~~ 82, wherein the data transfer control additionally transfers the user data in parallel to and from the host.

93 ~~153.~~ The memory system according to any one of claims ~~141~~ 79 - ~~144~~ 82, additionally comprising an erasing circuit that simultaneously erases the individual cells within individual designated blocks.

94 ~~154.~~ The memory system according to claim ~~153~~ 93, wherein the overhead data generated in the data transfer control and written into said at least one addressed block includes at least one of a group of an error correction code for the user data written into said at least one addressed block, an address of the individual said at least one addressed block, a map of defective cells within said at least one addressed block and a count related to a number of times that said at least one addressed block has been erased.